Script **generated by TTT**

Title: Petter: Programmiersprachen (12.11.2014)

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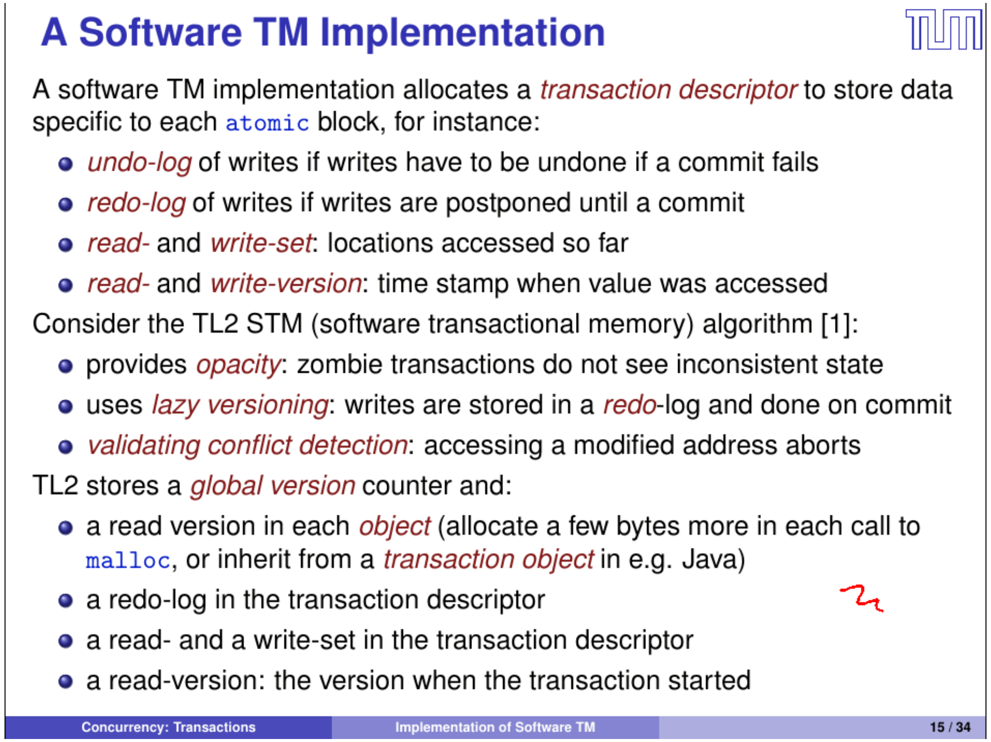


A Software TM Implementation

A software TM implementation allocates a *transaction descriptor* to store data specific to each `atomic` block, for instance:

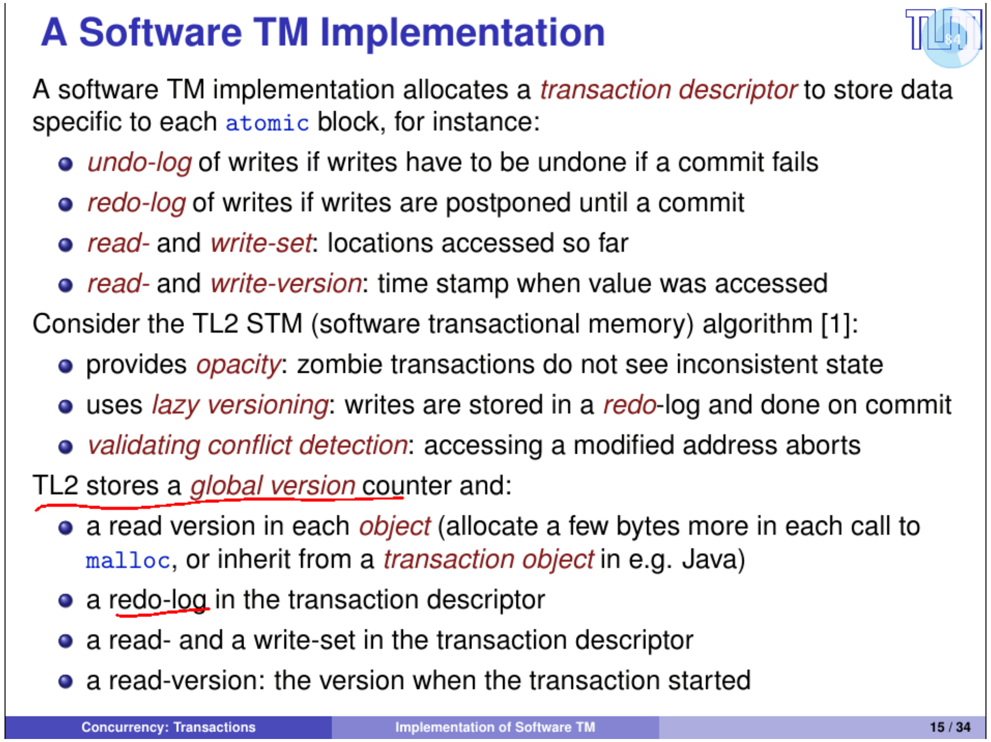
- *undo-log* of writes if writes have to be undone if a commit fails
- *redo-log* of writes if writes are postponed until a commit
- *read-* and *write-set*: locations accessed so far
- *read-* and *write-version*: time stamp when value was accessed

Consider the TL2 STM (software transactional memory) algorithm [1]:

- provides *opacity*: zombie transactions do not see inconsistent state
- uses *lazy versioning*: writes are stored in a *redo*-log and done on commit
- *validating conflict detection*: accessing a modified address aborts

TL2 stores a *global version* counter and:

- a read version in each *object* (allocate a few bytes more in each call to `malloc`, or inherit from a *transaction object* in e.g. Java)
- a redo-log in the transaction descriptor
- a read- and a write-set in the transaction descriptor
- a read-version: the version when the transaction started



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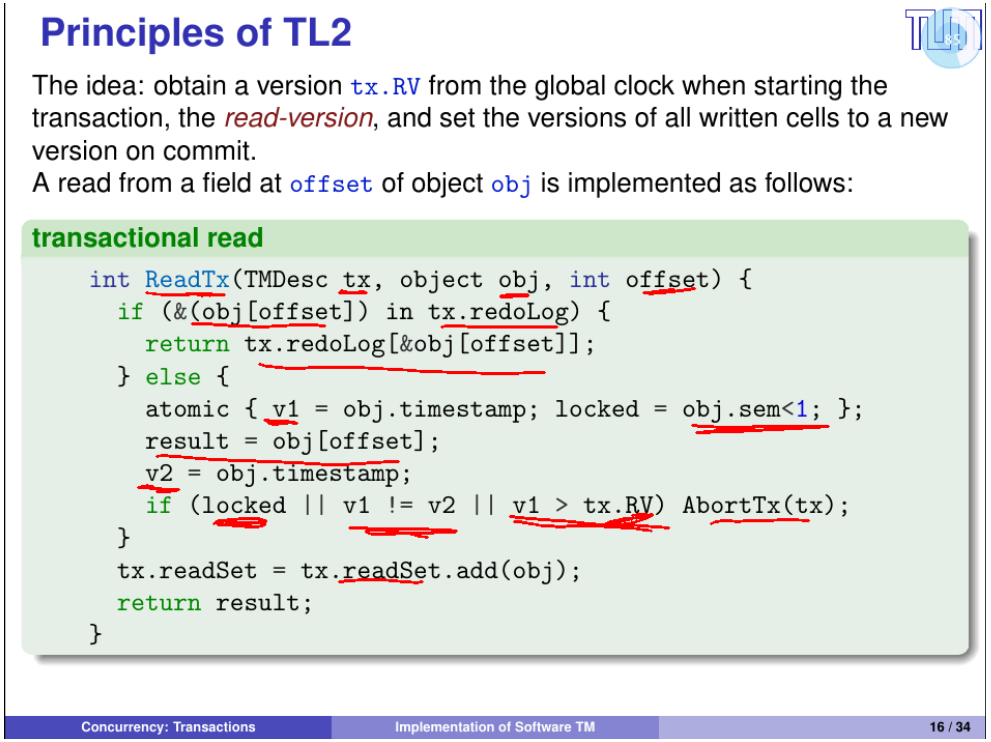

Principles of TL2

The idea: obtain a version `tx.RV` from the global clock when starting the transaction, the *read-version*, and set the versions of all written cells to a new version on commit.
A read from a field at `offset` of object `obj` is implemented as follows:

transactional read

```
int ReadTx(TMDesc tx, object obj, int offset) {
  if (&(obj[offset]) in tx.redoLog) {
    return tx.redoLog[&obj[offset]];
  } else {
    atomic { v1 = obj.timestamp; locked = obj.sem<1; };
    result = obj[offset];
    v2 = obj.timestamp;
    if (locked || v1 != v2 || v1 > tx.RV) AbortTx(tx);
  }
  tx.readSet = tx.readSet.add(obj);
  return result;
}
```

Committing a Transaction

A transaction can succeed if none of the read locations has changed:

committing a transaction

```
bool CommitTx(TMDesc tx) {
  foreach (e in tx.writeSet)
    if (!try_wait(e.obj.sem)) goto Fail;
  WV = FetchAndAdd(&globalClock);
  foreach (e in tx.readSet)
    if (e.obj.version > tx.RV) goto Fail;
  foreach (e in tx.redoLog)
    e.obj[e.offset] = e.value;
  foreach (e in tx.writeSet) {
    e.obj = WV; signal(e.obj.sem);
  }
  return true;
Fail:
  // signal all acquired semaphores
  return false;
}
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lock+update+version+unlock

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`WriteTx` is simpler: add or update the location in the redo-log.

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General Challenges when using TM

Executing `atomic` blocks by repeatedly trying to executing them non-atomically creates new problems:

- a transaction might unnecessarily be aborted
  - the granularity of what is locked might be too large
  - a TM implementation might impose restrictions:

```
// Thread 1                      // Thread 2
atomic { // clock=12
  ...
                                 atomic {
                                   WriteTx(&x,0) = 42; // clock=13
                                 }

  int r = ReadTx(&x,0);
} // tx.RV=12/=clock (X)
```

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- TM system should figure out which memory locations must be logged
- danger of live-locks: transaction B might abort A which might abort B . . .

Integrating Non-TM Resources

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- *Prohibit It.* Certain constructs do not make sense. Use compiler to reject these programs.
- *Execute It.* I/O operations may only happen in some runs (e.g. file writes usually go to a buffer). Abort if I/O happens.
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⇝ currently best to use TM only for memory; check if TM supports irrevocable transactions

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- additional hardware to track read- and write-sets

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   - provides *strong isolation*

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Intel provides two software interfaces to TM:

1. Restricted Transactional Memory (RTM)
2. Hardware Lock Elision (HLE)

Restricted Transactional Memory (Intel)

Provides new instructions XBEGIN, XEND, XABORT, and XTEST:

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- XTEST checks if the processor is executing transactionally

The instruction XBEGIN can be implemented as a C function:

```
int data[100]; // shared
void update(int idx, int value) {
  if(_xbegin()==-1) {
      data[idx] += value;
      _xend();
    } else {
      // transaction failed
    }
}
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⇝ user must provide fall-back code

Considerations for the Fall-Back Path

Consider executing the following code in parallel with itself:

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Problem:

- if the fall-back code is executed, it might be interrupted by the transaction
- the write in the fall-back path thereby overwrites the value of the transaction

Protecting the Fall-Back Path

Use a lock to prevent the transaction from interrupting the fall-back path:

```
int data[100]; // shared
int mutex;
void update(int idx, int value) {
  if(_xbegin()==-1) {
      data[idx] += value;
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    } else {
      wait(mutex);
      data[idx += value];
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- fall-back path may not run in parallel with others ✓
- ⚠ transactional region may not run in parallel with fall-back path

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void update(int idx, int value) {
  if(_xbegin()==-1) {
      if (mutex>0) _xabort();
      data[idx] += value;
      _xend();
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      wait(mutex);
      data[idx += value]
      signal(mutex);
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}
```

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Implementing RTM using the Cache

Transactional operation:

- augment each cache line with an extra bit T

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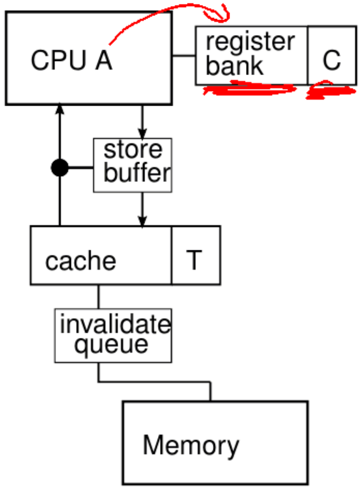

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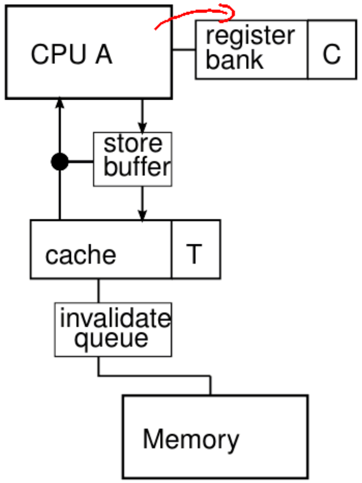

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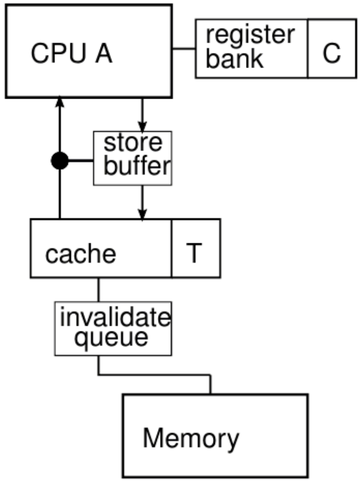

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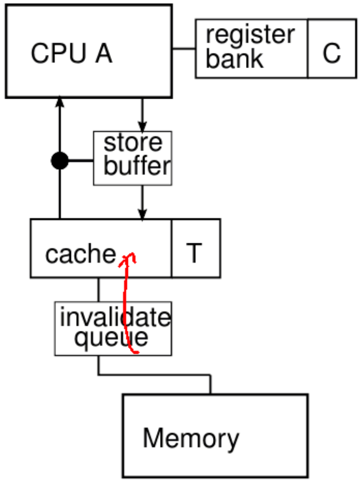

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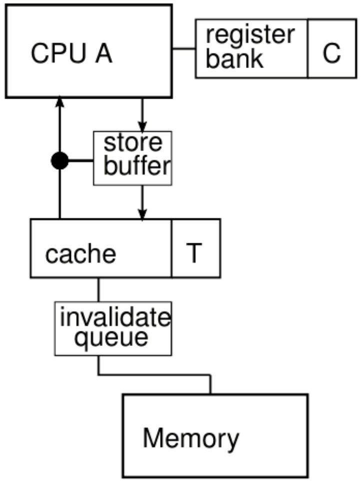

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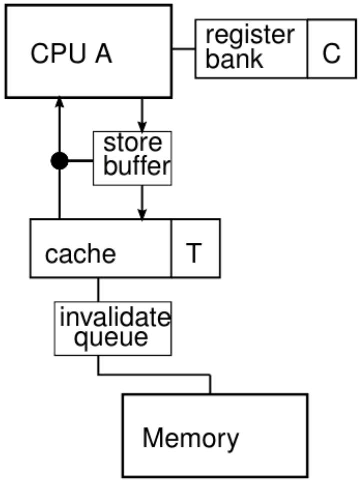

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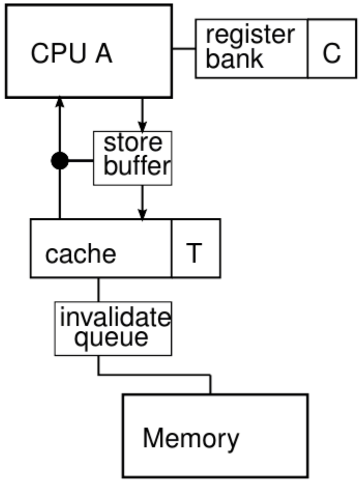

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- XCOMMIT decrement C and, if $C = 0$, clear all T flags

Illustrating Transactions

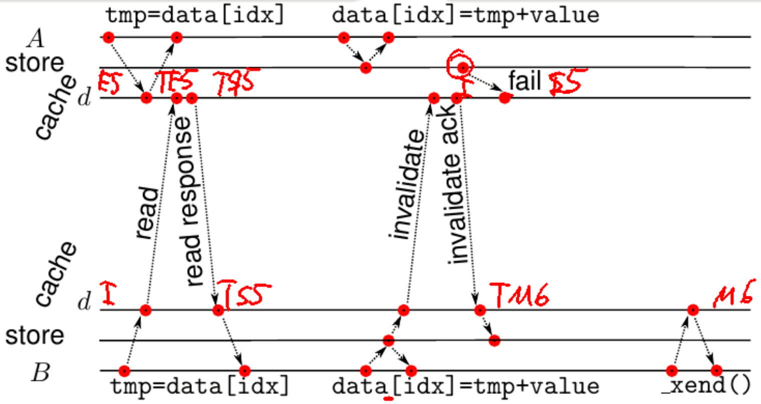
Augment MESI state with extra bit T per cache line. CPU A: E5, CPU B: I

Thread A

```
int tmp = data[idx];
data[idx] = tmp+value;
_xend();
```

Thread B

```
int tmp = data[idx];
data[idx] = tmp+value;
_xend();
```



Common Code Pattern for Mutexes

Using HTM in order to implement mutex:

```
int data[100]; // shared
int mutex;
void update(int idx, int value) {
  if(_xbegin()==-1) {
    if (mutex>0) _xabort();
      data[idx] += value;
      _xend();
  } else {
      wait(mutex);
      data[idx] += value;
      signal(mutex);
  }
}
```

```
void update(int idx, int val) {
  lock(mutex);
  data[idx] += val;
  unlock(mutex);
}
void lock(int mutex) {
  if(_xbegin()==-1)
    if (mutex>0) _xabort();
    else return;
  wait(mutex);
}
void unlock(int mutex) {
    if (mutex>0) signal(mutex);
    else _xend();
}
```

- the critical section may be executed without taking the lock (the lock is *elided*)
- as soon as one thread conflicts, it aborts, takes the lock in the fallback path and thereby aborts all other transactions that have read mutex

Hardware Lock Elision

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⇝ provide special handling in hardware: HLE

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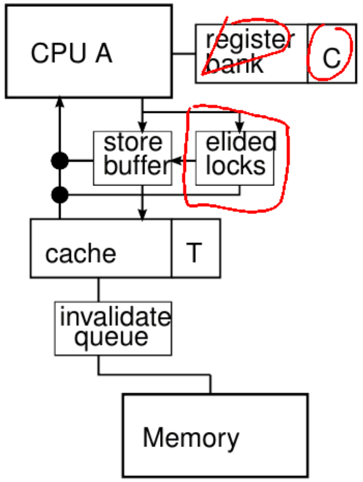

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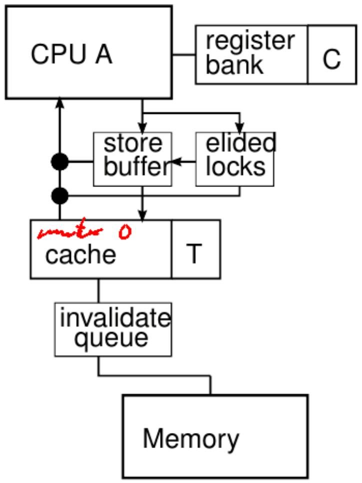

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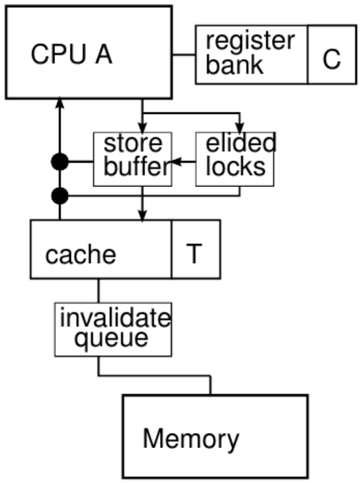

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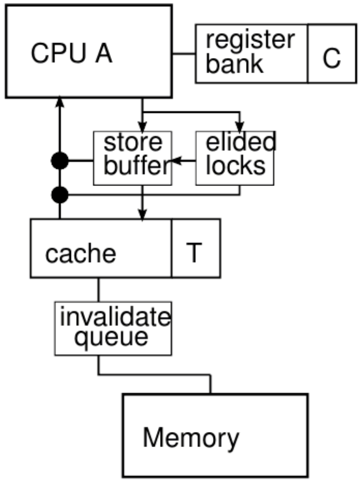

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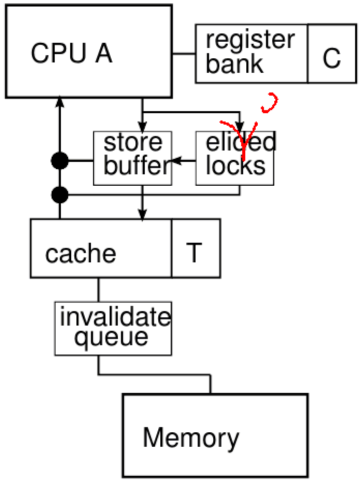

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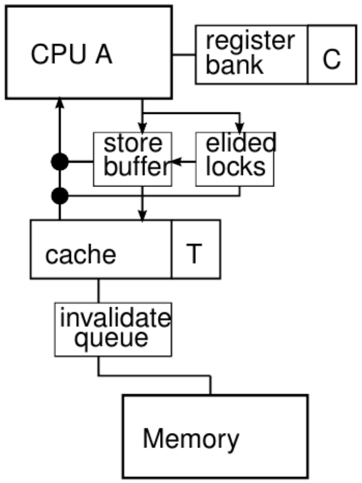

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- on XRELEASE on the same lock, decrement C and, if $C = 0$, clear T flags and elided locks buffer (thus, all locks contain the value 1 stored in the cache)

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Transactional memory aims to provide atomic blocks for general code:

- frees the user from deciding how to lock data structures
- compositional way of communicating concurrently
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The devil lies in the details:

- semantics of *explicit HTM* and *STM* transactions quite subtle when mixing with non-TM (*weak* vs. *strong isolation*) Opacity
- *single-lock atomicity* and *transactional sequential consistency* semantics
- STM not the right tool to synchronize threads without shared variables
- TM providing *opacity* (serializability) requires *eager conflict detection* or *lazy version management*

Devils in *implicit* HTM:

- RTM requires a fall-back path
- no progress guarantee
- HLE can be implemented in software using RTM

TM in Practice

Availability of Software TM:

- converting each read/write access to shared variables is tedious
- GCC can translate accesses in __transaction_atomic regions into library calls
- the library libitm may provide different STM algorithms
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Use of hardware lock elision is limited:

- allows to easily convert existing locks
- `pthread` locks in `glibc` use RTM `https://lwn.net/Articles/534758/`:
  - allows implementation of back-off mechanisms
  - HLE only special case of general lock
- implementing monitors is challenging
  - lock count and thread id may lead to conflicting accesses
  - in `pthreads`: error conditions often not checked anymore

Outlook

Several other principles exist for concurrent programming:

1. non-blocking message passing (the actor model)
   - a program consists of actors that send messages
   - each actor has a queue of incoming messages
   - messages can be processed and new messages can be sent
   - special filtering of incoming messages
   - *example:* Erlang, many add-ons to existing languages
2. blocking message passing (CSP, π-calculus, join-calculus)
   - a process sends a message over a channel and blocks until the recipient accepts it
   - channels can be send over channels (π-calculus)
   - *examples:* Occam, Occam-π, Go
3. (immediate) priority ceiling
   - declare *processes* with priority and *resources* that each process may acquire
   - each resource has the maximum (ceiling) priority of all processes that may acquire it
   - a process' priority at run-time increases to the maximum of the priorities of held resources
   - the process with the maximum (run-time) priority executes

References

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1. `http://software.intel.com/en-us/blogs/2013/07/25/fun-with-intel-transactional-synchronization-extensions`
2. `http://www.realworldtech.com/haswell-tm/4/`